

REMARKS

Favorable reconsideration of this application, in light of the following discussion, is respectfully requested. After entry of the foregoing amendment, Claims 1, 3-5, 7, 9-11, and 13 remain pending in the present application. No new matter has been added.

By way of summary, the Office Action presents the following issues: Claims 1-7 and 9 stand rejected under 35 U.S.C. § 103(a) as obvious over Vis (U.S. Patent No. 7,012,772) in view of Fermo et al. ("Simplified Volterra Filters for Acoustic Echo Cancellation in GSM receivers" (2000) (unpublished manuscript, on file with the Office), hereinafter "Fermo") and Terrell et al. (Digital Signal Processing: Principals, Devices and Applications 86 (N. B. Jones & J. D. McK. Watson eds., Institution of Engineering and Technology 1990) (1982), hereinafter "Terrell"); Claim 10 stands rejected under 35 U.S.C. § 103(a) as obvious over Vis in view of Fermo, Terrell, and McIntyre et al. (U.S. Patent No. 5,422,805, hereinafter "McIntyre"); and Claims 11-12 were indicated as allowable if rewritten in independent form.

ALLOWABLE SUBJECT MATTER

Applicant thanks Examiner Vlahos for the indication of allowable subject matter. Applicant has amended independent Claims 1, 4-5, and 9 to recite allowable features of dependent Claim 12. Further, Applicant has rewritten allowable Claim 11 in independent form.

ABSTRACT

Applicant has deleted the Abstract and submits herewith a new Abstract. No new matter has been added.

REJECTIONS UNDER 35 U.S.C. § 103

Claim 10 stands rejected under 35 U.S.C. § 103(a) as obvious over Vis in view of Fermo, Terrell, and McIntyre. Applicant has rewritten Claim 10 in independent form and has amended that claim for further clarity, thereby more clearly patentably defining over the applied references.

Amended Claim 10 recites a signal processing apparatus, where

a quadratic section of said second-order Volterra filter . . . includes a plurality of multiplication units configured to multiply a first input signal with a second input signal to produce a product signal, . . . a remaining one of said plurality of multiplication units being configured to employ a signal delayed a preset time from said first input signal, as said second input signal, . . .

the remaining one of said plurality of multiplication units including,

a shifter configured to left-shift the product signal to produce the signal output from the remaining one of said plurality of multiplication units, and

a multiplier configured to multiply the signal output from the remaining one of said plurality of multiplication units with a preset coefficient.

Applicant respectfully submits that Vis, Fermo, Terrell, and McIntyre fail to disclose or suggest those features.

The Office concedes that “neither Vis, nor Fermo or [Terrell] expressly disclose: wherein said multiplication unit further includes a shifter configured to left-shift the product signal to produce the signal output [from] said multiplication unit.”¹ To remedy this deficiency, the Office relies on McIntyre.

McIntyre concerns an apparatus for multiplying two numbers using signed arithmetic, in which “Multiplier/MAC 33 multiplies together . . . quantities at its X and Y inputs to

¹ Office Action at 10, ll. 7-9.

provide a . . . product.”² According to McIntyre, “Multiplier/MAC 33 also scales (left-shifts) the fractional product by one bit.”³

That is, McIntyre merely describes left-shifting a product. Applicant respectfully submits that McIntyre fails to disclose or suggest “a shifter configured to left-shift the product signal to produce the signal output from the remaining one of said plurality of multiplication units, and a multiplier configured to multiply the signal output from the remaining one of said plurality of multiplication units with a preset coefficient,” as recited in amended Claim 10.

It is therefore submitted that Vis, Fermo, Terrell, and McIntyre, taken alone or in combination, fail to disclose or suggest “a shifter configured to left-shift the product signal to produce the signal output from the remaining one of said plurality of multiplication units, and a multiplier configured to multiply the signal output from the remaining one of said plurality of multiplication units with a preset coefficient,” as recited in amended Claim 10. Accordingly, it is respectfully submitted that independent Claim 10 patentably distinguishes over any proper combination of Vis, Fermo, Terrell, and McIntyre.

² McIntyre, col. 9, ll. 9-11.

³ Id., col. 9, ll. 11-13.

CONCLUSION

Consequently, in view of the present amendment and in light of the foregoing comments, it is respectfully submitted that the present application is patentably distinguished over the cited art and is in condition for allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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